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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,565	09/12/2003	Howard Rhodes	M4065.0570/P570-A	5308
24998	7590	01/24/2005	EXAMINER	
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP			VU, QUANG D	
2101 L Street, NW			ART UNIT	
Washington, DC 20037			PAPER NUMBER	
			2811	

DATE MAILED: 01/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/660,565

Applicant(s)

RHODES ET AL.

Examiner

Quang D. Vu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 September 2004.  
 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 90 and 93-141 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
 6) ☒ Claim(s) 90 and 93-141 is/are rejected.  
 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) ☐ All b) ☐ Some \* c) ☐ None of:  
 1. ☐ Certified copies of the priority documents have been received.  
 2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_.  
 4) ☐ Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_.  
 5) ☐ Notice of Informal Patent Application (PTO-152)  
 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 122, 125, 126, 127, 128, 129, 137, 140 and 141 are rejected under 35

U.S.C. 102(b) as being anticipated by US Patent No. 6,204,524 to Rhodes.

Regarding claim 122, Rhodes (figures 1-14) teaches a method of forming an imager comprising the steps of:

providing a semiconductor substrate (116, 120) having a doped layer (120) of a first conductivity type (p type);

forming a field oxide region (115) in the semiconductor substrate;

forming a photosensor (125) including a charge collection region (155) of a second conductivity type (n type), the charge collection region (155) being provided in the doped layer (120);

forming a floating diffusion region (130) for receiving charge from the charge collection region (155); and

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forming a charge storage capacitor (162) over the semiconductor substrate (116, 120) so that one electrode (156) of the storage capacitor (162) is connected to the floating diffusion region (130) by an electrical contact (150).

Regarding claim 125, Rhodes teaches the charge storage capacitor (162) is formed partially over the field oxide region (115) and partially over an active area of the photosensor (125).

Regarding claim 126, Rhodes teaches the other electrode (160) of the charge storage capacitor (162) is connected to ground (column 8, lines 17-18).

Regarding claim 127, Rhodes teaches the other electrode (156) of the charge storage capacitor (162) is connected to a gate of a transistor (102).

Regarding claim 128, Rhodes teaches the transistor is part of a three-transistor cell (photogate transistor [125], transfer transistor [128], reset transistor [132]).

Regarding claim 129, Rhodes teaches the transistor is part of a four-transistor cell (photogate transistor [125], transfer transistor [128], reset transistor [132], source follower transistor [136]).

Regarding claim 137, Rhodes (figures 1-14) teaches a method of forming an imager comprising the steps of:

providing a semiconductor substrate (116, 120) having a doped layer (120) of a first conductivity type (p type);

forming a field oxide region (115) in the semiconductor substrate;

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forming a photosensor (125) including a charge collection region (155) of a second conductivity type (n type), the charge collection region (155) being provided in the doped layer (120);

forming a floating diffusion region (130) for receiving charge from the charge collection region (155);

connecting an electrode of a first charge storage capacitor (capacitors [64, 74]; figure 1) to the floating diffusion region (130) by a first electrical contact (42) (floating diffusion region [130] connects to a readout circuit [60]; column 7, lines 42-54); and

connecting an electrode of a second charge storage capacitor (162) to the charge collection region (110) by a second electrical contact (150).

Regarding claim 140, Rhodes teaches the second charge storage capacitor (162) is formed such that the extent of the charge storage capacitor (162) overlies an active area of the photodiode (photodiode; column 2, lines 29-31).

Regarding claim 141, Rhodes teaches a first portion (left portion of [162]) of the second charge storage capacitor (162) is formed over the field oxide region (115) and wherein a second portion (right portion of [162]) of the second charge storage capacitor (162) is formed over an active area of the photodiode (photodiode; column 2, lines 29-31).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 90, 93-101, 104-119, 123 and 130-136 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,204,524 to Rhodes in view of US Patent No. 6,300,662 to Doyle et al.

Regarding claim 90, Rhodes (figures 1-14) teaches a method of forming a CMOS imager comprising the steps of:

providing a semiconductor substrate (116, 120) having a doped layer (120) of a first conductivity type (p type);

forming a first doped region (155) of a second conductivity type (n type) in the doped layer (120), the first doped region (155) being adjacent a field oxide region (115);

forming a charge storage capacitor (162); and

forming a contact (150) between the first doped region (155) and the charge storage capacitor (162).

Rhodes differs from the claimed invention by not showing the entire extend of the charge storage capacitor overlies the field oxide region. However, Doyle et al. (figure 7B) teach the entire extend of the charge storage capacitor (C<sub>2</sub>), which overlies the field oxide region (40). Therefore, it would have been obvious to one having ordinary skill in the art at the time the

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invention was made to incorporate the teaching of Doyle et al. into the device taught by Rhodes in order to improve the capacity of the charge storage capacitor.

Regarding claim 93, the combined device shows the charge storage capacitor (Rhodes; 162) is formed by forming a first conductive layer (Rhodes; 156) over the substrate (Rhodes; 116, 120) including the field oxide region (Rhodes; 115); forming a dielectric layer (Rhodes; 158) over the first conductive layer (Rhodes; 156); and forming a second conductive layer (Rhodes; 160) over the dielectric layer (Rhodes; 158).

Regarding claim 94, the combined device shows the first (Rhodes; 156) and second (Rhodes; 160) conductive layers are independently selected from W (tungsten) (Rhodes; column 9, lines 54 – 60; column 10, lines 15 – 18).

Regarding claim 95, the combined device shows forming an element of the CMOS imager simultaneously with forming the storage capacitor (Rhodes; 162).

Regarding claim 96, the combined device shows the element is a transistor gate (Rhodes; 125).

Regarding claim 97, the combined device shows connecting an electrode of the storage capacitor (Rhodes; 162) to the transistor gate (Rhodes; 125).

Regarding claim 98, the combined device shows the element is a transfer gate (Rhodes; 128).

Regarding claim 99, the combined device shows connecting an electrode of the storage capacitor (Rhodes; 162) to the transfer gate (Rhodes; 128).

Regarding claim 100, the combined device shows the element is a source follower gate (Rhodes; 136).

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Regarding claim 101, the combined device shows connecting an electrode of the storage capacitor (Rhodes; 162) to the source follower gate (Rhodes; 136).

Regarding claim 104, the combined device shows forming a second doped region (Rhodes; 126) of the second conductivity type (n type) in the doped layer (Rhodes; 120) spaced from the first doped region (Rhodes; 155) to transfer charge from a charge collection area; forming a third doped region (Rhodes; 130) of the second conductivity type in the doped layer (Rhodes; 120) spaced from the second doped region (Rhodes; 110) wherein the third doped region effectuates the transfer of charge to a readout circuit; and forming a fourth doped region (Rhodes; 134) of the second conductivity type in the doped layer (Rhodes; 120) spaced from the third doped region (Rhodes; 130) wherein the fourth doped region is a drain for a reset transistor for the CMOS imager.

Regarding claim 105, the combined device shows the first conductivity type is p-type (Rhodes; p type; column 7, lines 24-26), and the second conductivity type is n-type (Rhodes; n type; column 7, lines 32-34).

Regarding claim 106, the combined device shows forming a photogate (Rhodes; 102) over the doped layer (Rhodes; 120) between the first (Rhodes; 155) and second (Rhodes; 126) doped regions.

Regarding claim 107, the combined device shows connecting an electrode of the storage capacitor (Rhodes; 162) to the photogate (Rhodes; 102).

Regarding claim 108, Rhodes (figures 1-14) teaches a method of forming a CMOS imager having improved charge storage comprising the steps of:

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providing a semiconductor substrate (116, 120) having a doped layer (120) of a first conductivity type (p type);

forming a field oxide region (115) within the semiconductor substrate;

forming a first conductive layer (156) over the field oxide region (115) and the substrate (116, 120);

forming an insulating layer (158) over the first conductive layer (156);

forming a second conductive layer (160) over the insulating layer (158);

patterning the first conductive layer (156), the insulating layer (158) and the second conductive layer (160) to form a storage capacitor (162) and an electrical element of the CMOS imager.

Rhodes differs from the claimed invention by not showing the entire extent of the storage capacitor is formed over the field oxide region. However, Doyle et al. (figure 7B) teach the entire extend of the charge storage capacitor ( $C_2$ ), which overlies the filed oxide region (40). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Doyle et al. into the device taught by Rhodes in order to improve the capacity of the charge storage capacitor.

Regarding claim 109, the combined device shows forming a first doped region (Rhodes; 155) of a second conductivity type (n type) in the doped layer (Rhodes; 120) and adjacent the field oxide region (Rhodes; 115); forming a second doped region (Rhodes; 126) of the second conductivity type (n type) in the doped layer (Rhodes; 120) spaced from the first doped region (Rhodes; 155); forming a third doped region (Rhodes; 130) of the second conductivity type (n type) in the doped layer (Rhodes; 120) spaced from the second doped region (Rhodes; 126) and

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adjacent the electrical element (Rhodes; gate [128]); and forming a fourth doped region (Rhodes; 134) of the second conductivity type (n type) in the doped layer (Rhodes; 120) spaced from the third doped region (Rhodes; 130).

Regarding claim 110, the combined device shows the first conductivity type is p-type (Rhodes; p type; column 7, lines 24-26), and the second conductivity type is n-type (Rhodes; n type; column 7, lines 32-34).

Regarding claim 111, the combined device shows the first doped region, the second doped region, the third doped region and the fourth doped region are doped at a dopant concentration of from about  $1 \times 10^{15}$  ions/cm<sup>2</sup> to about  $1 \times 10^{16}$  ions/cm<sup>2</sup> (Rhodes; column 9, lines 20 – 24).

Regarding claim 112, the combined device shows the element is a transistor gate (Rhodes; 125).

Regarding claim 113, the combined device shows connecting an electrode of the storage capacitor (Rhodes; 162) to the transistor gate (Rhodes; 125).

Regarding claim 114, the combined device shows the electrical element is a reset transistor gate (Rhodes; 132).

Regarding claim 115, the combined device shows connecting an electrode of the storage capacitor (Rhodes; 162) to the reset transistor gate (Rhodes; 132).

Regarding claim 116, the combined device shows the element is a source follower gate (Rhodes; 136).

Regarding claim 117, the combined device shows connecting an electrode of the storage capacitor (Rhodes; 162) to the source follower gate (Rhodes; 136).

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Regarding claim 118, the combined device shows the electrical element is a row select transistor gate (Rhodes; 138).

Regarding claim 119, the combined device shows connecting an electrode of the storage capacitor (Rhodes; 162) to the row select transistor gate (Rhodes; 138).

Regarding claim 123, Rhodes differs from the claimed invention by not showing the entire extend of the charge storage capacitor overlies the field oxide region. However, Doyle et al. (figure 7B) teach the entire extend of the charge storage capacitor ( $C_2$ ), which overlies the filed oxide region (40). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Doyle et al. into the device taught by Rhodes in order to improve the capacity of the charge storage capacitor.

Regarding claim 130, Rhodes (figures 1-14) teaches a method of forming an imager comprising the steps of:

- providing a semiconductor substrate (116, 120) having a doped layer (120) of a first conductivity type (p type);

- forming a field oxide region (115) in the semiconductor substrate;

- forming a photodiode (p-n junction photodiode; column 2, lines 29-31) in the doped layer (120);

- forming a charge storage capacitor (162); and

- connecting an electrode of a charge storage capacitor (162) to the photodiode by an electrical contact (contact [150]).

Rhodes differs from the claimed invention by not showing the entire extend of the charge storage capacitor overlies the field oxide region. However, Doyle et al. (figure 7B) teach the

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entire extend of the charge storage capacitor ( $C_2$ ), which overlies the filed oxide region (40).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Doyle et al. into the device taught by Rhodes in order to improve the capacity of the charge storage capacitor.

Regarding claim 131, the combined device shows the other electrode (Rhodes; 160) of the charge storage capacitor (Rhodes; 162) is connected to ground (Rhodes; column 8, lines 17-18).

Regarding claim 132, the combined device shows the other electrode (Rhodes; 156) of the charge storage capacitor (Rhodes; 162) is connected to a gate of a transistor (Rhodes; gate [102]).

Regarding claim 133, the combined device shows the transistor is a transfer transistor (Rhodes; 128).

Regarding claim 134, the combined device shows the transistor is a source follower transistor (Rhodes; 136).

Regarding claim 135, the combined device shows the transistor is a row select transistor (Rhodes; 138).

Regarding claim 136, the combined device shows the transistor is part of a three-transistor cell (Rhodes; photogate transistor [125], transfer transistor [128], reset transistor [132]).

5. Claims 102, 103, 120 and 121 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes in view of Doyle et al., and further in view of US Patent No. 6,262,703 to Perner.

Regarding claim 102, the disclosures of Rhodes and Doyle et al. are discussed as applied to claims 90, 93-101 and 104-107 above.

The combined device differs from the claimed invention by not showing the element is a gate of a global shutter transistor. However, Perner teaches the global transistor (column 4, lines 22-24). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Perner into the device taught by Rhodes and Doyle et al. because it is desirable to transmit the high signals of the transistor.

Regarding claim 103, the combined device shows connecting an electrode of the storage capacitor to the gate of the global shutter transistor (Perner; global transistor).

Regarding claim 120, the disclosures of Rhodes and Merrill et al. are discussed as applied to claims 108-119 above.

The combined device differs from the claimed invention by not showing the element is a gate of a global shutter transistor. However, Perner teaches the global transistor (column 4, lines 22-24). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Perner into the device taught by Rhodes and Doyle et al. because it is desirable to transmit the high signals of the transistor.

Regarding claim 121, the combined device shows connecting an electrode of the storage capacitor to the gate of the global shutter transistor (Perner; global transistor).

6. Claims 124 and 139 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,204,524 to Rhodes in view of US Patent No. 6,741,283 to Merrill et al.

Regarding claim 124, Rhodes differs from the claimed invention by not showing the entire extent of the charge storage capacitor overlies an active area of the photosensor. Merrill et al. (figures 7A-B) teach the entire extent of the charge storage capacitor (124), which is formed

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over an active area in the substrate. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Merrill et al. into the device taught by Rhodes in order to improve the capacity of the charge storage capacitor.

Regarding claim 139, Rhodes differs from the claimed invention by not showing a first portion of the first charge storage capacitor is formed over the field oxide region, and wherein a second portion of the first charge storage capacitor is formed over an active area of the photodiode. However, Merrill et al. (figures 7A-B) teach the portion of the charge storage capacitor (124) is formed over the field oxide region (114), and the portion of the charge storage capacitor (124) is formed over an active area of the photodiode. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Merrill et al. into the device taught by Rhodes in order to improve the capacity of the charge storage capacitor.

7. Claim 138 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,204,524 to Rhodes in view of US Patent No. 6,744,084 to Fossum.

Regarding claim 138, Rhodes differs from the claimed invention by not showing the first charge storage capacitor is formed such that the extent of the charge storage capacitor overlies an active area of the photodiode. However, Fossum (figure 7) teaches the charge storage capacitor (171) is formed such that the extent of the charge storage capacitor overlies an active area of the photodiode (188). Therefore, it would have been obvious to one having ordinary skill in the art

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at the time the invention was made to incorporate the teaching of Fossum into the device taught by Rhodes in order to improve the capacity of the charge storage capacitor.

### ***Response to Arguments***

Applicant's arguments with respect to claims 90 and 93-141 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D. Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

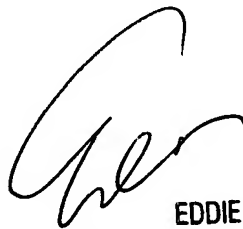
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv

January 6, 2005



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